

Pattern Marker and Bit Error Counter Option for the SIA-3000™

**Comprehensive
jitter analysis
on only the
data stream**

**Bit Error
Counting**

The tremendous increase in data traffic and transmission speeds has fueled the demand for better high-speed networking components and systems. Ensuring the signal integrity of these devices has never been more important. Traditionally, performing jitter measurements on systems is difficult because it requires the use of a bit clock or trigger, which is typically unavailable. The Pattern Marker option for the SIA-3000 enables jitter compliance measurements on systems without the need for a bit clock or pattern trigger thereby providing a simple and easy to use setup.

The Pattern Marker option enables the user to simply input a data stream with a repeating pattern into an SIA-3000 channel card and obtain quantitative information on DJ, RJ, PJ, DCD&ISI and their contribution to Total Jitter. The Pattern Marker option produces a pattern marker from a unique portion of the pattern or by counting a user specified number of data edges. The pattern marker option decreases the measurement time compared to using a pattern generator pattern marker or pattern trigger because it generates a marker for every pattern repeat. For example, a typical data analysis on a PRBS $2^{15}-1$ pattern at 1.5 Gb/s will take ~2 minutes with the pattern marker option but over 20 minutes using a pattern marker from a pattern generator with a marker density of 1/16. Additionally, the pattern marker card, along with *VISI™* software, automatically locates the marker in a low transition density region of the pattern eliminating the need to use delay lines to place the pattern marker in an optimal location ensuring reliable and repeatable results.

The Pattern Marker option also has the capability to detect bit errors in the pattern. The user can view the errors and their location in the pattern as illustrated in Figures 1(a) and (b). The ability to detect bit errors provides additional information about low probability errors, pattern dependent errors and is useful in jitter tolerance measurements to determine the BER. Bit error counting can be performed at distinct frequencies in pattern match mode.

Typical applications include jitter measurements on Host Bus Adapters, Host Channel Adapters, Target Channel Adapters, GBICs, IC's as well as other systems and components.

Standard SIA-3000 configurations consist of one Pattern Marker card and 2, 4 or 5-channel cards. Other configurations are available upon request.

PM50 Performance Specifications

Data rates for pattern match mode	1.0625, 1.25, 1.5, 2.125, 2.5, and bit error counting	3.0, 3.125, 3.1875 Gb/s \pm 0.1%	
Data rate range for edge count mode	Continuous up to 5.0 Gb/s		
DCD&ISI Noise floor	\leq 1% added to individual channel card specification		
Pattern requirements for	Pattern must be 10, 20, 40 bits or pattern match mode		divisible by 40. 40-bit pattern match word must contain a K28.5 character.
Pattern requirements for Bit Error counter	\geq 40 bits		
Pattern requirements for edge count mode	None		



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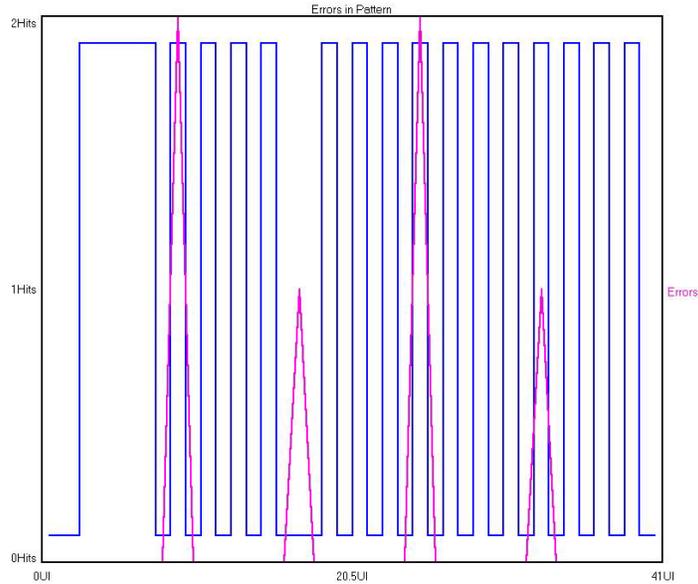
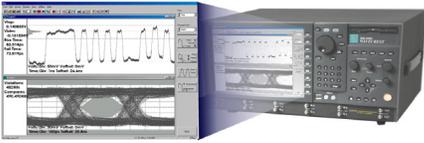


Figure 1(a) shows a plot of the pattern and the number of errors for each bit in the pattern. In this example there are six bit errors at four different bits in the pattern.

Pattern Marker Summary

Pattern Marker PM1	Mode Pattern Match	Standard 2X FC 2.125 Gb/s
Pattern File idle.ptn	Total Delay 0s	Edge Count 16
20-bit Errors 6	Total Compares 29.267258e9	BER 2.050072e-010
Pattern Repeat	Frame Number	20-bit Data In Error
596859123	0	00111110 ⁰ 1010100010
615776191	0	00111110 ⁰ 1010100010
634502766	0	0011111010 101010 ⁰ 1010
652095529	1	1010101010 10 ⁰ 0101010
669976830	1	1010 ⁰ 01010 1010101010
685542942	1	1010 ⁰ 01010 1010101010

Figure 1(b) shows the summary of the Bit Error Count information. This table shows the number of bit errors, BER, pattern repeat of the error, 20 bit frame in the pattern where the error occurred and the specific bit that was in error (indicated by a ^ above the number).



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